AMENDMENTS TO THE CLAIMS

This listing of Claims shall replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-52. (Cancelled)

53. (Currently Amended) A system comprising:

a plurality of memory resources;

a plurality of peripheral resources;

a plurality of processors;

a memory controller coupled to said plurality of processors and said plurality of memory resources, wherein said memory controller comprises a first resource controller operable to control access by said plurality of processors to said plurality of memory resources using a hardware semaphore unit, wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of memory resources, ~~and~~ wherein said memory controller is further operable to enable each processor of said plurality of processors to simultaneously access a respective portion of a memory resource of said plurality of memory resources, and wherein said memory controller is further operable to enable each of said plurality of processors to have priority access to a respective instruction memory of a plurality of instruction memories; and

a peripheral controller coupled to said plurality of processors and said plurality of peripheral resources, wherein said peripheral controller comprises a second resource controller operable to control access by said plurality of processors to said plurality of peripheral resources using said hardware semaphore unit, and wherein said second resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources.

54. (Previously Presented) The system of Claim 53 further comprising:

a timer component coupled to said memory controller and said peripheral controller, said timer component operable to control timing of said memory controller and said peripheral controller.

55. (Previously Presented) The system of Claim 53, wherein said first resource controller is further operable to enable each of said plurality of processors to simultaneously access a respective memory resource of said plurality of memory resources.

56. (Previously Presented) The system of Claim 53, wherein said second resource controller is further operable to enable each of said plurality of processors to simultaneously access a respective peripheral resource of said plurality of peripheral resources.

57. (Previously Presented) The system of Claim 53, wherein said memory controller and said peripheral controller are further operable to enable each processor of said plurality of processors to perform, in parallel, respective portions of a plurality of tasks.

58. (Previously Presented) The system of Claim 53, wherein said plurality of processors are operable to negotiate for access to at least one shared resource using said hardware semaphore unit, wherein said at least one shared resource is selected from a group consisting of at least one memory resource of said plurality of memory resources and at least one peripheral resource of said plurality of peripheral resources.

59. (Previously Presented) The system of Claim 58, wherein said hardware semaphore unit is further operable to enable said plurality of processors to communicate with one another.

60. (Previously Presented) The system of Claim 58, wherein said access to said at least one shared resource is determined based upon information selected from a group consisting of: a chronological ordering of requests for a shared resource, a round-robin access arbitration scheme; a predetermined priority assignment of a given processor to at least one given shared resource; and a predetermined priority assignment of a given processor to at least one given shared resource for a predetermined period of time.

61. (Previously Presented) The system of Claim 53, wherein said plurality of memory resources, said plurality of peripheral resources, said plurality of processors, said memory controller, and said peripheral controller comprise components of a portable electronic device.

62. (Currently Amended) A component for negotiating access to a plurality of shared resources, said component comprising:

a memory controller coupled to said plurality of processors and said plurality of memory resources, wherein said memory controller comprises a first resource controller operable to control access by said plurality of processors to said plurality of memory resources using a hardware semaphore unit, wherein said first resource controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of memory resources, ~~and~~ wherein said memory controller is further operable to enable each processor of said plurality of processors to simultaneously access a respective portion of a memory resource of said plurality of memory resources, and wherein said memory controller is further operable to enable each of said plurality of processors to have priority access to a respective instruction memory of a plurality of instruction memories; and

a peripheral controller coupled to said plurality of processors and said plurality of peripheral resources, wherein said peripheral controller comprises a second resource controller operable to control access by said plurality of processors to said plurality of peripheral resources using said hardware semaphore unit, and wherein said second resource controller is further operable

to implement respective buses for coupling said plurality of processors to said plurality of peripheral resources.

63. (Previously Presented) The component of Claim 62 further comprising:

a timer component coupled to said memory controller and said peripheral controller, said timer component operable to control timing of said memory controller and said peripheral controller.

64. (Previously Presented) The component of Claim 62, wherein said first resource controller is further operable to enable each of said plurality of processors to simultaneously access a respective memory resource of said plurality of memory resources.

65. (Previously Presented) The component of Claim 62, wherein said second resource controller is further operable to enable each of said plurality of processors to simultaneously access a respective peripheral resource of said plurality of peripheral resources.

66. (Previously Presented) The component of Claim 62, wherein said memory controller and said peripheral controller are further operable to enable each processor of said plurality of processors to perform, in parallel, respective portions of a plurality of tasks.

67. (Previously Presented) The component of Claim 62, wherein said plurality of processors are operable to negotiate for access to at least one shared resource using said hardware semaphore unit, wherein said at least one shared resource is selected from a group consisting of at least one memory resource of said plurality of memory resources and at least one peripheral resource of said plurality of peripheral resources.

68. (Previously Presented) The component of Claim 67, wherein said hardware semaphore unit is further operable to enable said plurality of processors to communicate with one another.

69. (Previously Presented) The component of Claim 67, wherein said access to said at least one shared resource is determined based upon information selected from a group consisting of: a chronological ordering of requests for a shared resource; a round-robin access arbitration scheme; a predetermined priority assignment of a given processor to at least one given shared resource; and a predetermined priority assignment of a given processor to at least one given shared resource for a predetermined period of time.

70. (Previously Presented) The component of Claim 62, wherein said plurality of processors, said memory controller, and said peripheral controller comprise components of a portable electronic device.

71. (Currently Amended) A controller for negotiating access to a plurality of shared resources, said controller comprising:

a resource arbitration controller operable to control access by said plurality of processors to said plurality of shared resources using a hardware semaphore unit, wherein said resource arbitration controller is further operable to implement respective buses for coupling said plurality of processors to said plurality of shared resources, ~~and~~ wherein said resource arbitration controller is further operable to enable each processor of said plurality of processors to simultaneously access a respective portion of a shared resource of said plurality of shared resources, and wherein said resource arbitration controller is further operable to enable each of said plurality of processors to have priority access to a respective instruction memory of a plurality of instruction memories.

72. (Previously Presented) The controller of Claim 71, wherein said resource arbitration controller is further operable to control access of said plurality of processors to said plurality of shared resources based upon a respective priority value assigned to each of said plurality of processors.

73. (Previously Presented) The controller of Claim 72, wherein said respective priority value is assigned to each of said plurality of processors using a hardware semaphore unit.

74. (Previously Presented) The controller of Claim 71, wherein said plurality of shared resources are selected from a group consisting of at least one memory resource and at least one peripheral resource.

75. (Previously Presented) The controller of Claim 71, wherein said resource arbitration controller is further operable to enable each of said plurality of processors to simultaneously access a respective shared resource of said plurality of shared resources.

76. (Previously Presented) The controller of Claim 71, wherein said resource arbitration controller is further operable to enable each processor of said plurality of processors to perform, in parallel, respective portions of a plurality of tasks.